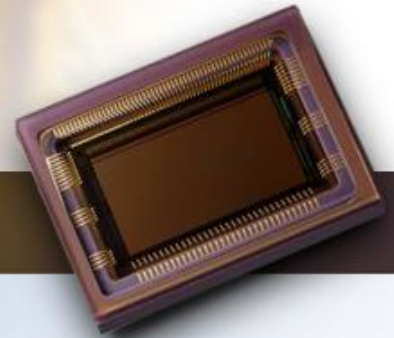


Global Shutter Image Sensors for Machine Vision Applications

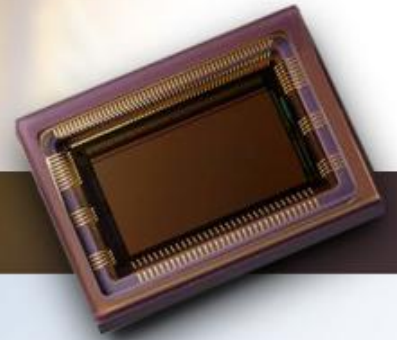
Image Sensors Europe 2010, 23-25 March 2010

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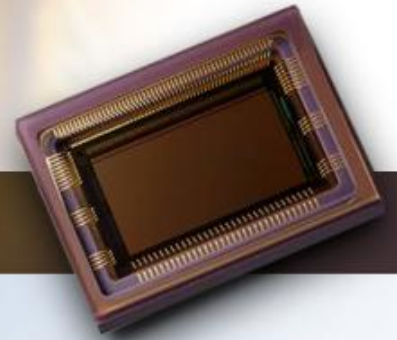
- Introduction
 - Machine vision sensor demands
 - Products definition
 - Current standard products
- Technology developments
 - Image sensor architecture
 - Low noise global shutter pixel
 - High speed column ramp ADCs
- Sensor characterization
 - Features and electro-optical specifications
 - Sample images & movie

Machine vision sensor demands



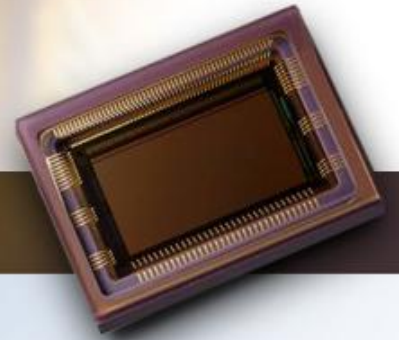
- Global shutter
 - Freeze fast moving object
 - No smear
- High sensitivity with low noise
 - Need enough image data with short exposure times
 - Low light sensitivity (apply gain if necessary)
 - Low parasitic light sensitivity (high shutter efficiency)
- Minimal 1.3 Mpixels, preferably higher
 - High detail in large field of view
 - Use digital zoom

Machine vision sensor demands



- High frame rate
 - Take a fast sequence of images to track movement
 - Exposure of an image while the previous is read out (pipelining)
- Ease of use
 - Implement on-board features
 - Programming of exposure and read-out modes using a SPI
- No image correction needed off-chip
 - No image post-processing needed
 - No dark frame subtraction (FPN correction)

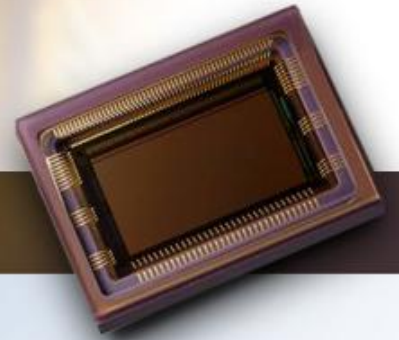
Definition of the products



- Talked to many potential customers
- Defined what was needed
- Proposed a specification list
- Feedback on product definition from beta customers
- Development of final product according to feedback

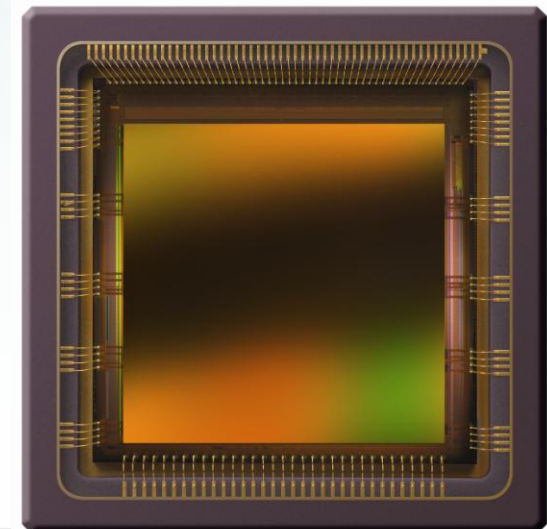
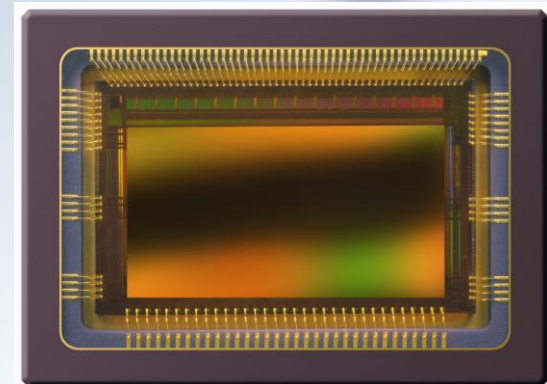
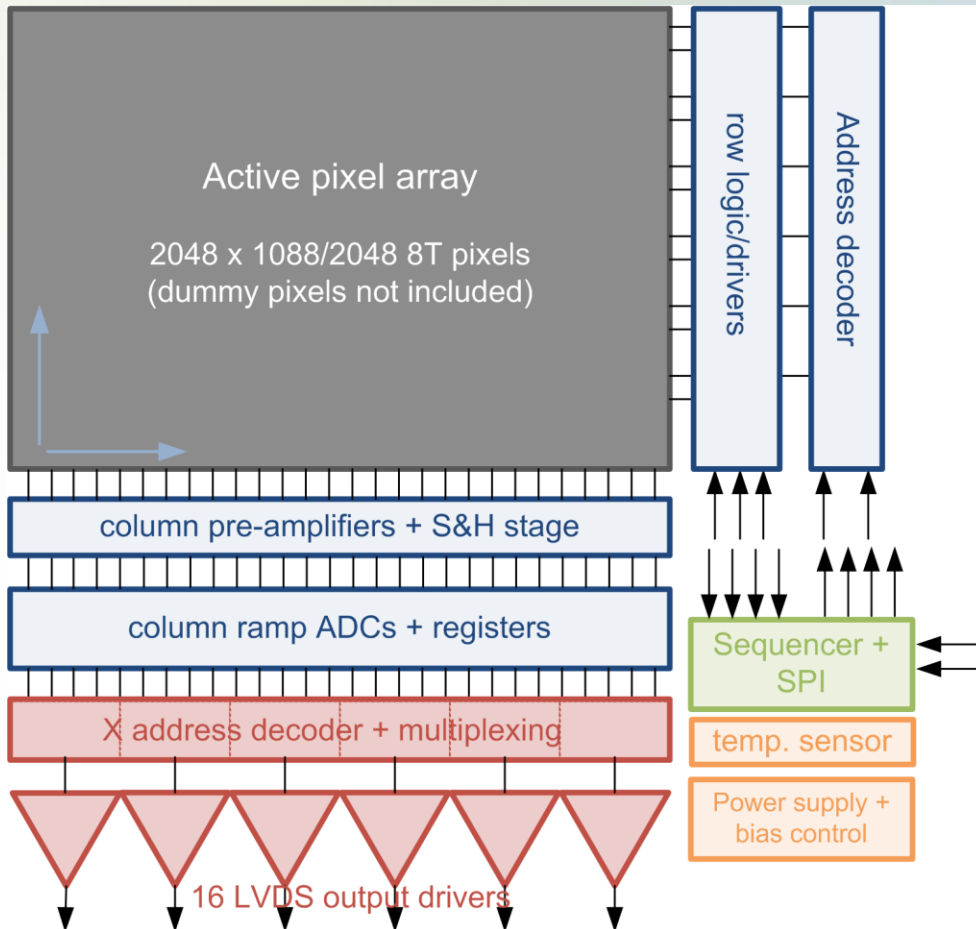
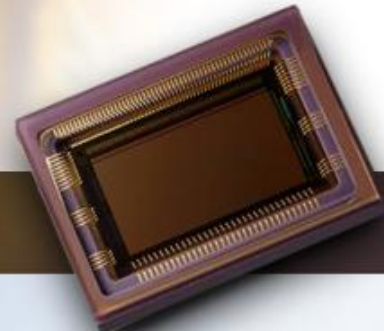
➔ Industry driven spec list!

Current products: 2 resolutions

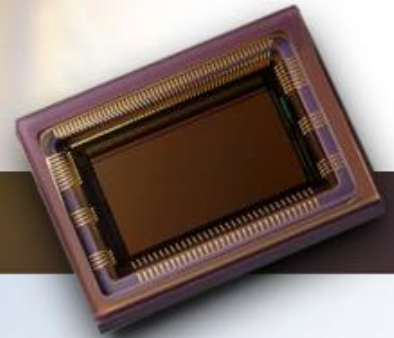


- CMV2000 – 2048 x 1088 pixels
 - Small form factor (2/3")
 - Support full HD
 - CMV4000 – 2048 x 2048 pixels
 - Square format for optimal lens area coverage
- ➔ Pin compatible with identical on-board features and electro-optical specifications

Sensor architecture

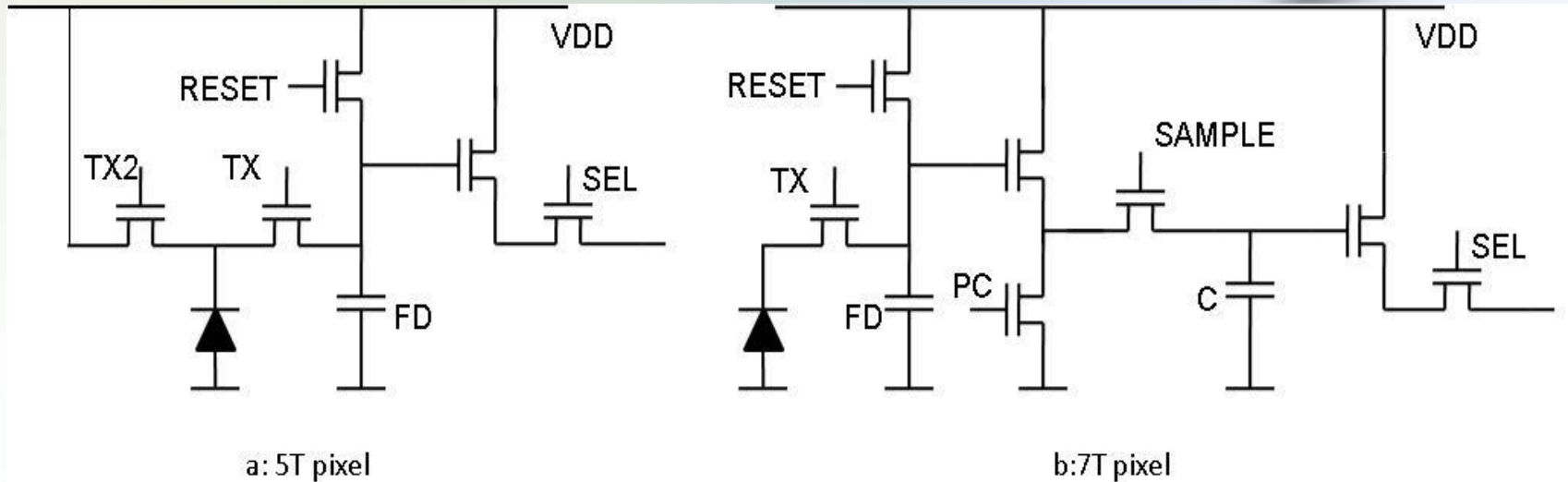
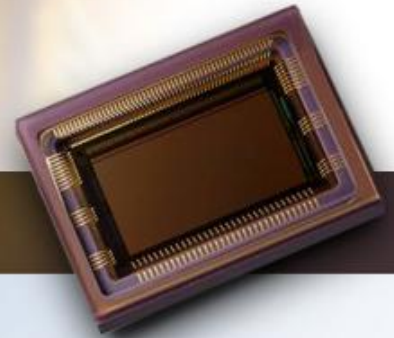


Architecture: highlights



- High speed
 - High speed column ADCs
 - Pipelined global shutter with CDS
 - 16 parallel high speed LVDS outputs (multiplexing possible)
- High sensitivity with low noise
 - Achieved by using a unique global shutter pixel with correlated double sampling (CDS)
 - High fill factor for high sensitivity
- Ease of use:
 - LVDS outputs
 - On-board sequencer
- Small form factor
 - 95 pin package (18.6mm x 13.5mm or 18.6mm x 18.6mm)

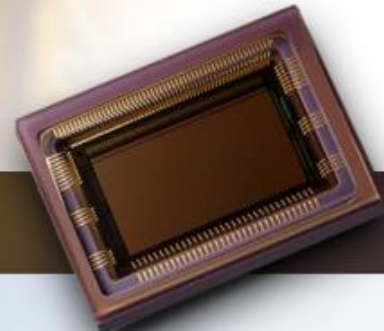
Pixel architecture: previous art



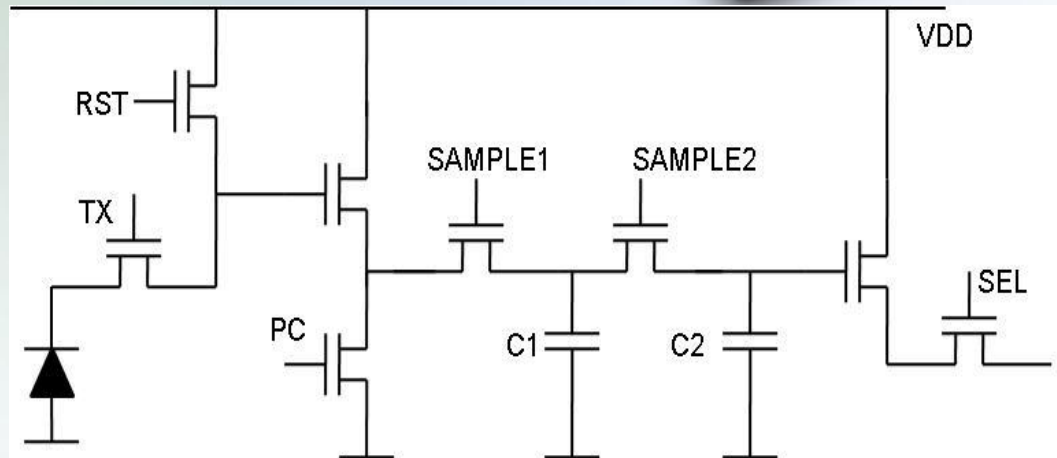
- Poor parasitic light sensitivity
- Reset noise is not cancelled
- Improved parasitic light sensitivity
- Reset noise is not cancelled

conversion gain (CvG) vs. dynamic range

Pixel architecture: CMOSIS 8T

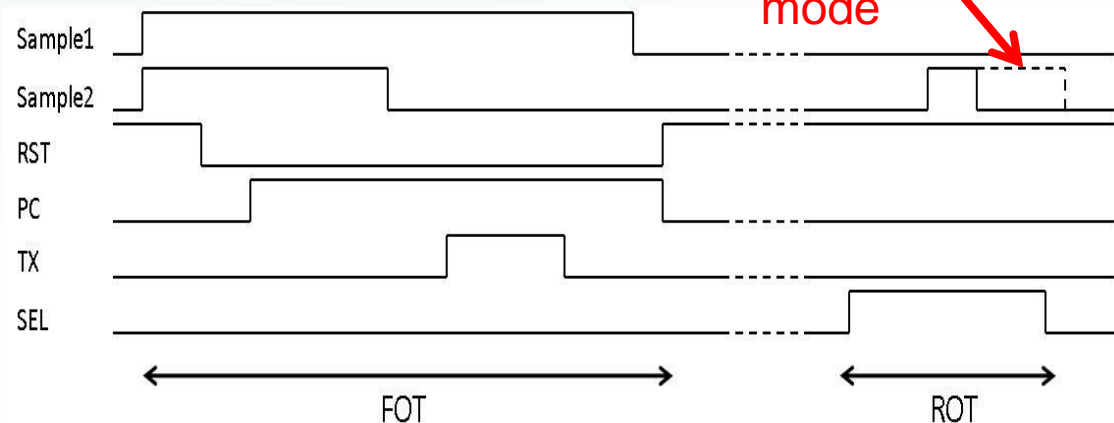


- Frame overhead time:
 - I. release RST
 - II. sample reset level on C2
 - III. charge transfer
 - IV. sample signal level on C1

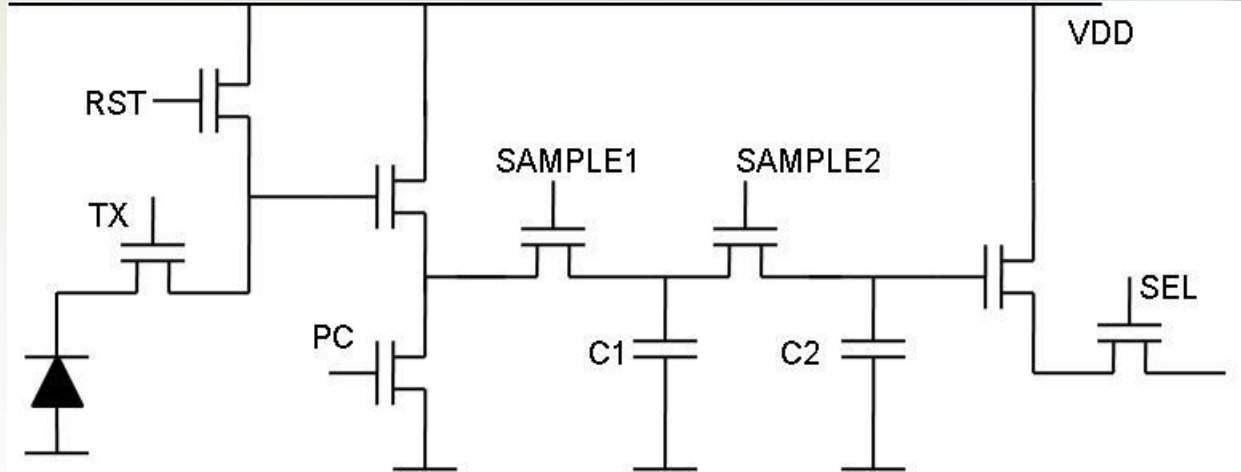
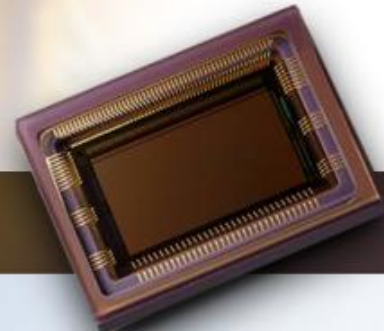


Low noise mode

- Row overhead time:
 - I. read reset level
 - II. short C1 & C2
 - III. read signal level



Pixel architecture: noise analysis



Pixel output after CDS:

$$\frac{V_{sig}}{2} + \sqrt{\frac{N^2(KTCs_2)}{4} + \frac{N^2(KTCs_1)}{4} + N^2(KTC's_2)}$$

Low noise mode:

$$\frac{V_{sig}}{2} + \sqrt{\frac{N^2(KTCs_2)}{4} + \frac{N^2(KTCs_1)}{4}}$$

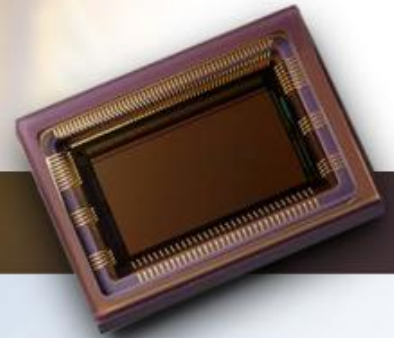


Assuming $C_1 = C_2 = C$

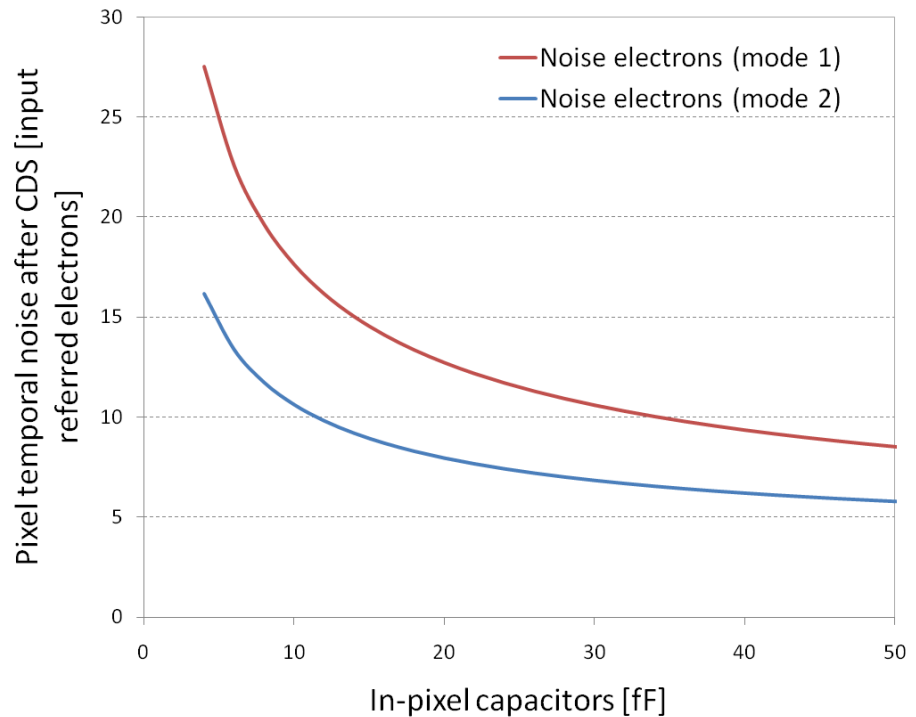
$$\frac{V_{sig}}{2} + \sqrt{1.5 * KT/C}$$

$$\frac{V_{sig}}{2} + \sqrt{0.5 * KT/C}$$

Pixel architecture: CMOSIS 8T

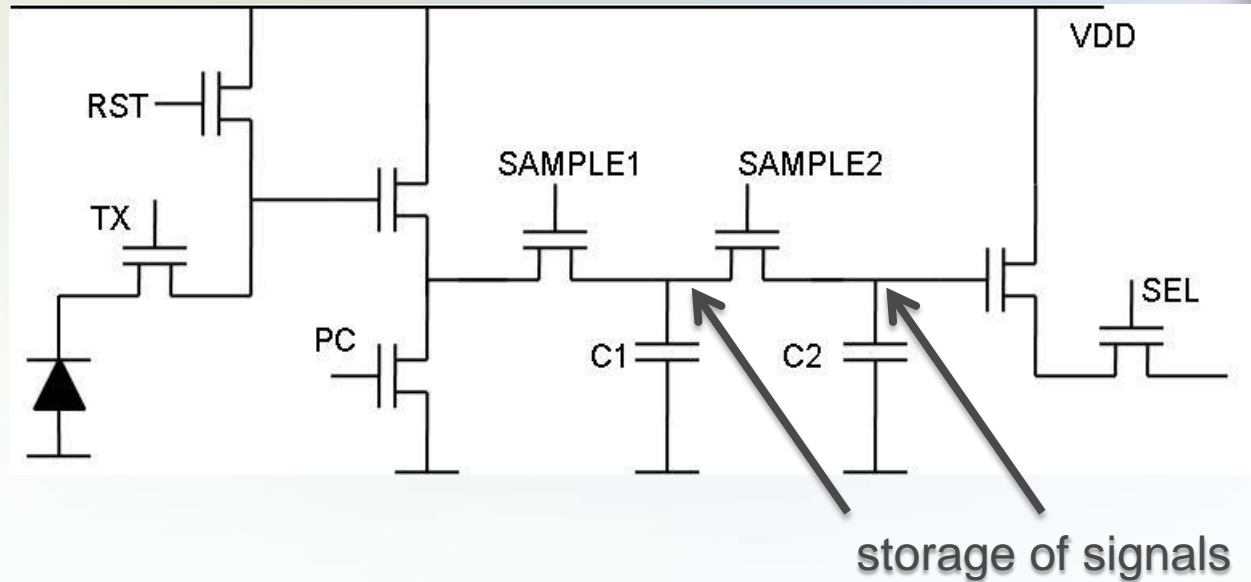
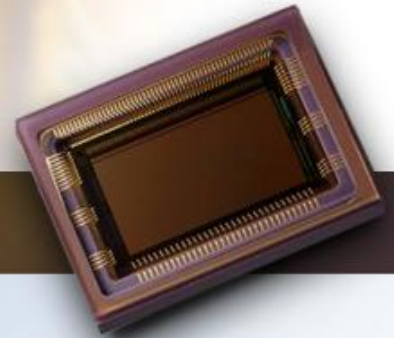


- Pixel noise (in voltage) only determined by C
- High C_vG desired
 - low noise (in input referred e^-)
 - better sensitivity
- Dynamic range (DR) independent of C_vG , only determined by swing and C
- Only small FWC is required for desired swing (i.e. dynamic range)



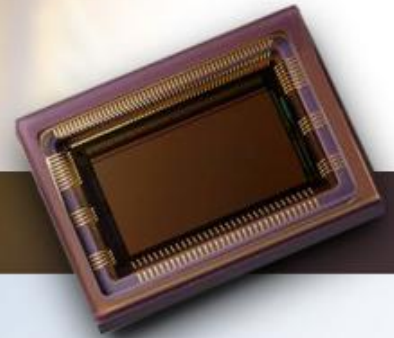
CDS in 8T pixel offers combination of low noise and high DR

Pixel architecture: PLS



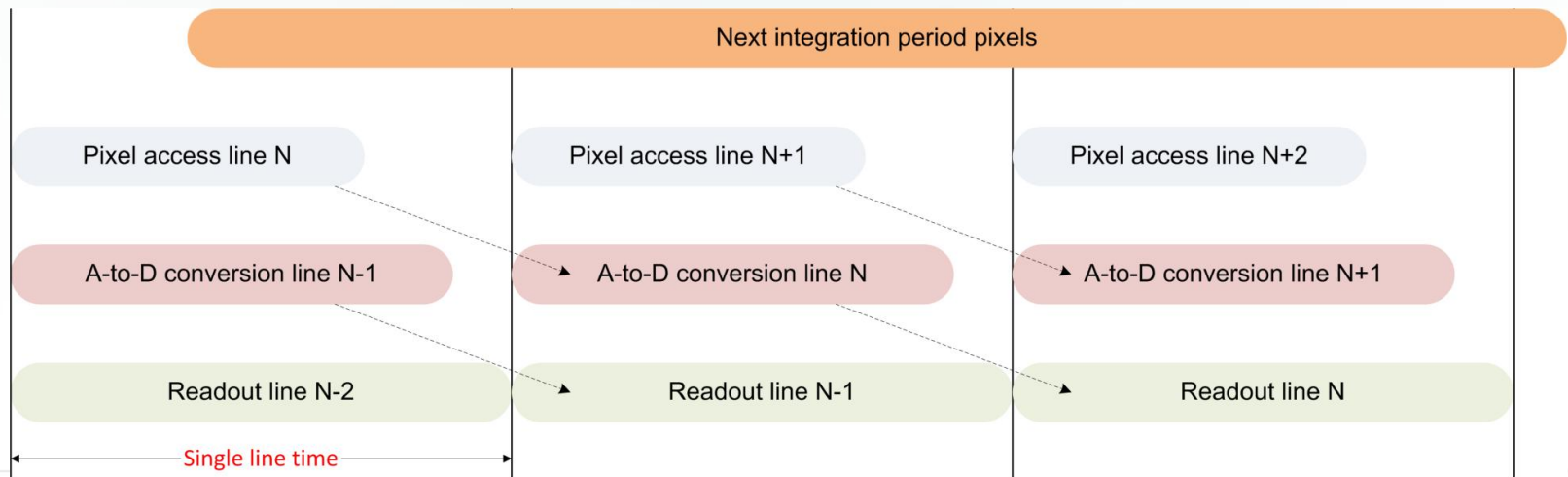
- Excellent shutter efficiency:
 - I. Storage C (C1 & C2) $\gg C_{FD}$
 - II. Storage capacitors have low parasitic light sensitivity
 - III. Parasitic leakage is cancelled by CDS operation
- Measured shutter efficiency: $> 99,998 \%$ (PLS $< 1/60000$)

Pipelined architecture

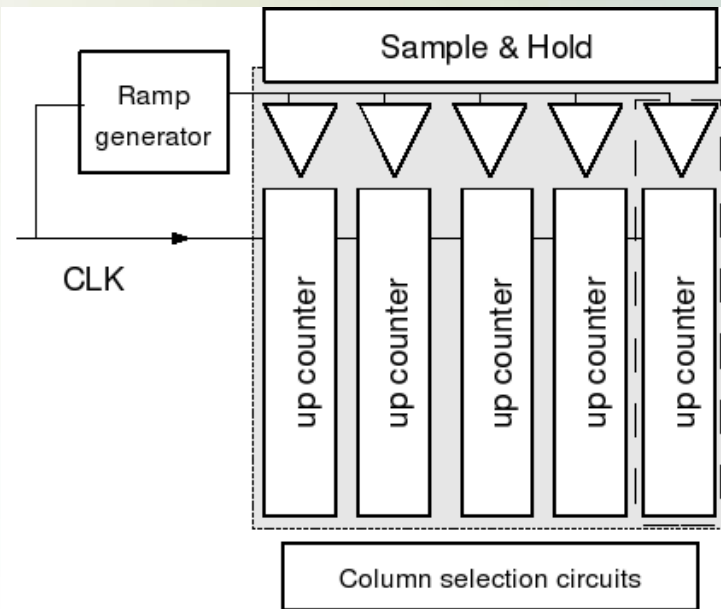
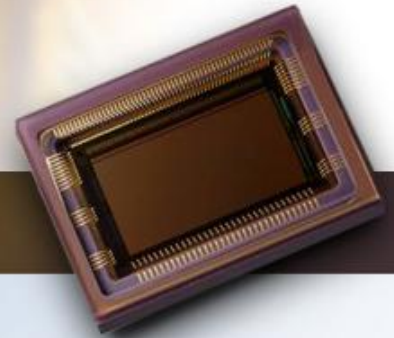


- Fully pipelined architecture

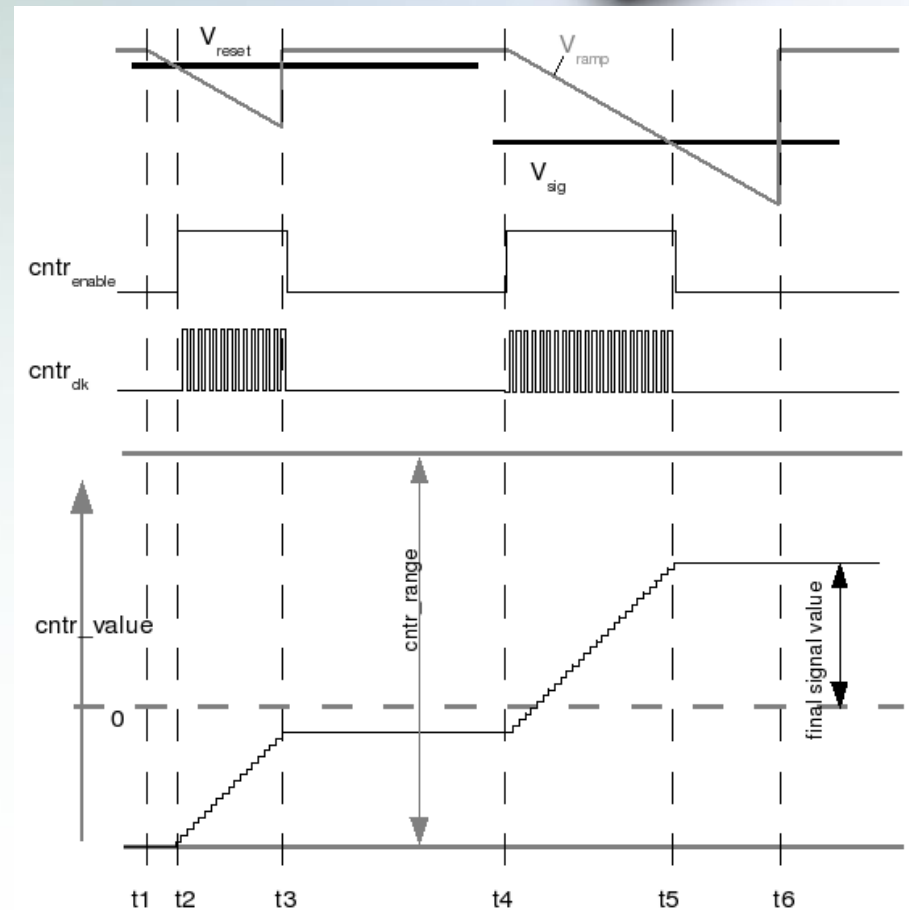
- Integration: next integration period starts while previous frame is being read out (pipelined global shutter)
- Readout processes are pipelined:
 - Pixel access and sampling
 - A-to-D conversion in column
 - Data readout to LVDS outputs



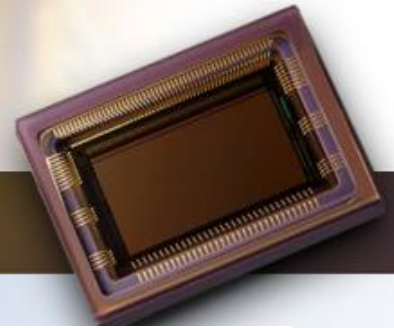
Column ramp ADCs



- Single distributed clock:
 - I. Clocked at 480 MHz
 - II. 10 bit: 2.7 $\mu\text{s}/\text{row}$
 - III. 12 bit: 10.8 $\mu\text{s}/\text{row}$

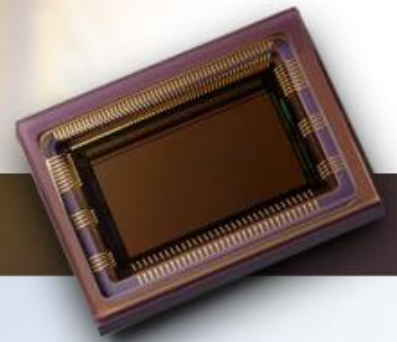


Sensor features



Feature	CMV2000	CMV4000
Resolution	2048 x 1088	2048 x 2048
Pixel size	5.5 um x 5.5 um	
Max. frame rate	340 fps	180 fps
Windowing	Row windowing (up to 8 separate ROIs)	
Image flipping	X and Y mirroring	
Output	16 LVDS outputs @ 480 MHz	
Multiplexing	To 8, 4 and 2 outputs	
ADC	10 bit, 12 bit at reduced frame rate	
High dynamic range	Multiple modes supported	
Programming	Over SPI interface	
Temperature control	On chip temperature sensor	
Sequencer	On chip timing generation	
Package	Ceramic μ PGA package (95 pins)	

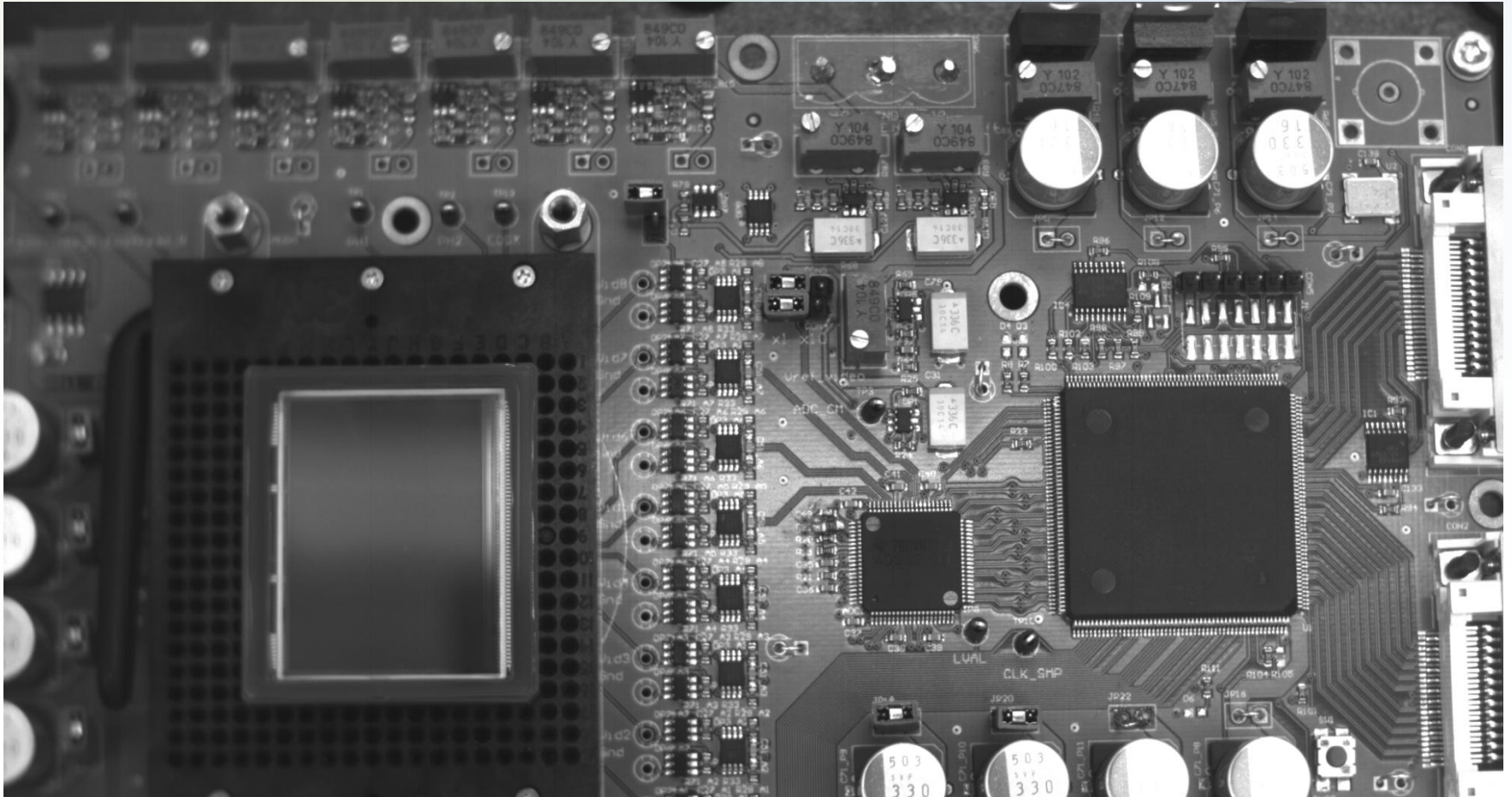
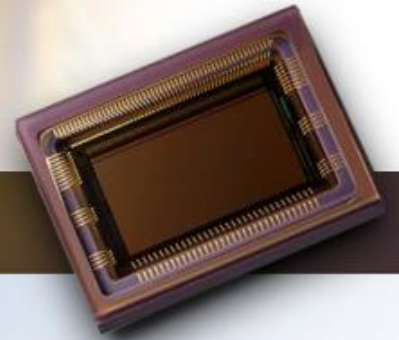
Sensor specifications



Specification	Value
Full Well charge	$> 12.5 \text{ Ke}^-$
Sensitivity	4.64 V/lux.s
Dark noise	$< 13 \text{ e}^-$
Conversion factor (10 bit mode)	$\sim 0.070 \text{ LSB/e}^-$
Dynamic range	$> 60 \text{ dB}$
Parasitic light sensitivity	$< 1/60000$
Dark current (10 bit mode)	22 LSB/s (@ room temp)
Fixed pattern noise (10 bit mode)	$< 1 \text{ LSB}$
Power consumption	600 mW

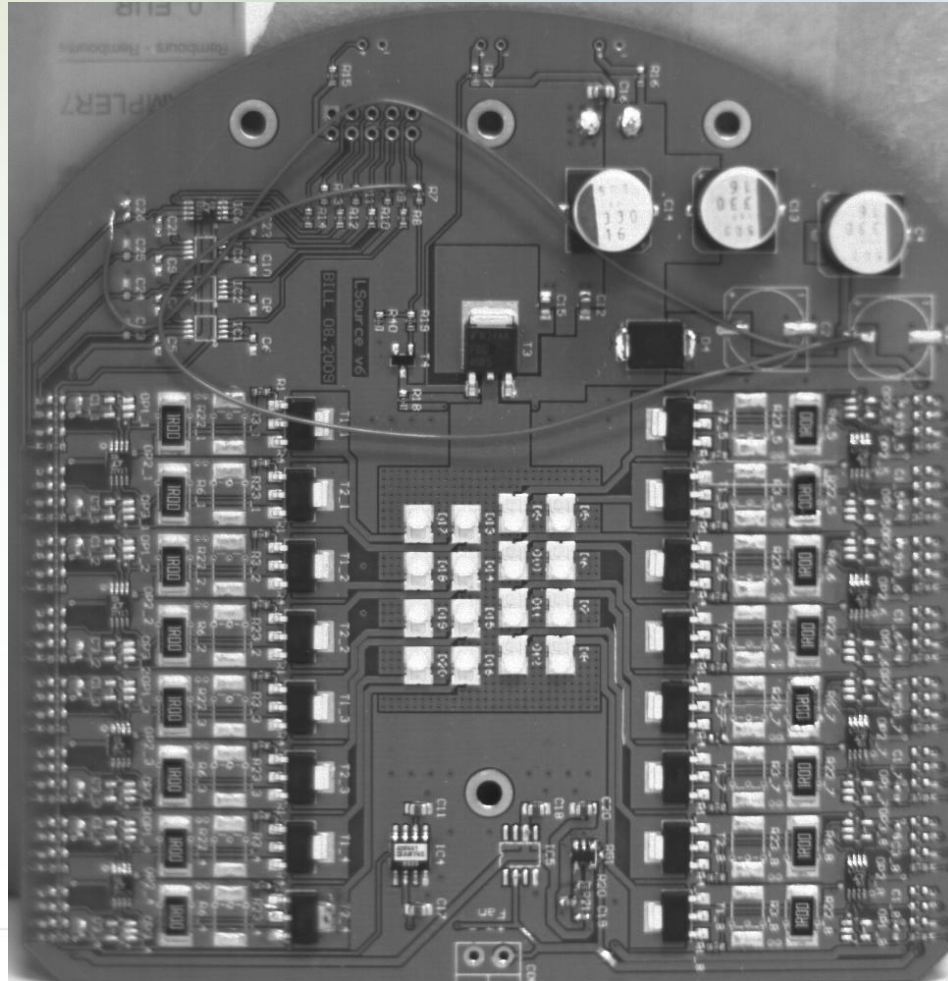
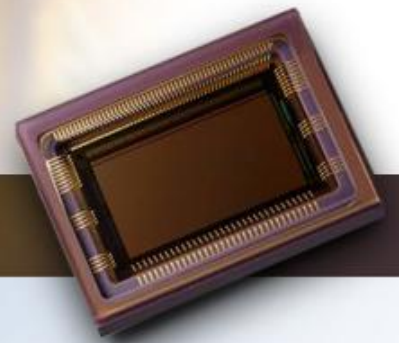
Example CMV2000

F/3, exposure 32ms, 300lux



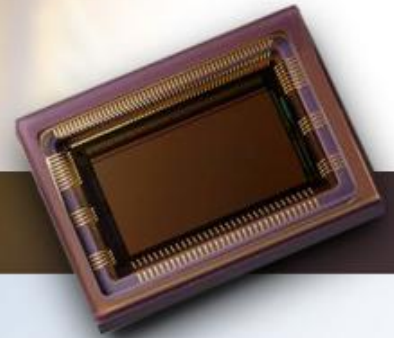
Example CMV4000

F/3, exposure 32ms, 300 lux

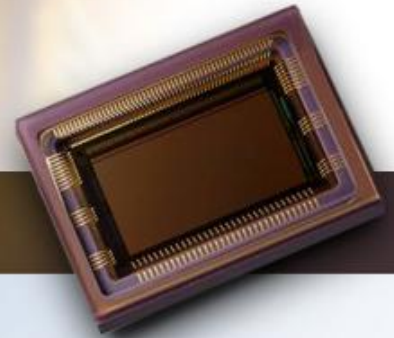


Movie example CMV2000

Full resolution, 280 fps (340 fps max)



Summary



- Industry driven feature and specification list
- CMOSIS has developed new technologies:
 - 8T pixel architecture allowing pipelined global shutter with CDS
 - CDS in 8T pixel brings combination of low noise (high sensitivity) and excellent dynamic range
 - Pixel with very high shutter efficiency
 - High speed pipelined readout architecture with column ramp ADCs
 - High frame rate combined with excellent image quality due to on-chip analog and digital CDS
- Future CMOSIS standard and custom designed sensors:
 - Pixel technology allows trade-off in terms of noise and SNR_{max} with high DR
 - Various pixel pitch and pixel resolution
 - Increase of I/O speed